Interlocking Conductor Method for Bonding Wafers to Produce Stacked Integrated Circuits

ABSTRACT

An integrated circuit wafer element and an improved method for bonding the same to produce a stacked integrated circuit. Plugs that extend from one surface of the wafer into the wafer are used to provide vertical connections and to bond the wafers together. A stacked integrated circuit is constructed by bonding the front side of a new wafer to a wafer in the stack and then thinning the backside of the new wafer to a thickness that leaves a portion of the plugs extending above the surface of the backside of the thinned wafer. The elevated plug ends can then be used to bond another wafer by bonding to pads on the front side of that wafer. The mating bonding pads can include depressed regions that mate to the elevated plug ends.